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PATENT & TRADEMARK OFFICE

ATTORNEY'S DOCKET NO.: S1022.81019US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Alexandre PONS and Christophe BERNARD		
Serial No.:	10/614,380	Patent No. 6,894,467 B2	
Filed:	July 7, 2003	Issued May 17, 2005	
For:	LINEAR VOLTAGE REGULATOR		
Examiner:	Adolf D. Berhane		
Art Unit:	2838	Confirmation No.:	7420

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
AUG 1 0 2005
of Correction

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Notification of Return of Papers
[X] Request for Certificate of Correction
[X] Copies of: Pages 9 and 10 of the Apl as Filed, Fig. 5 and Cols. 6 and 7 of issued U.S. Pat. No. 6,894,467
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646-8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on the 4 day of August, 2005.

Attorney Docket No.: S1022.80672US00
XNDD

Respectfully submitted,

Alexandre Pons et al., Applicant

By:
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PATENT NO.	PATENT DATE
	05/17/05
PATENTEE	
Alexandre Ponsand Christophe Bernard	

Paper No.:

MAILING DATE

Certificate
MAY 3 1 2005
of Correction

NOTIFICATION OF RETURN OF PAPERS
RE REQUEST FOR CERTIFICATE OF CORRECTION

The request for a Certificate of Correction in the above-identified patent is returned herewith, together with the PTOL-1050 (SB/44) forms (if submitted), for the reason(s) checked below.

☐ 1. The request is unsigned. The request must be properly signed before it will be considered.

☐ 2. The request does not specifically designate the column and line numbers wherein the errors appear in the patent. A substitute request providing this information is required, for proper consideration.

☐ 3. The FORM PTOL-1050 (SB/44) submitted with your request is not suitable for printing purposes. See the instructions on the blank Form PTO-1050, enclosed.

☐ 4. The Patent No., as shown on papers attach, appears to be incorrect, because:
- ☐ a. The Patent No. on the request and on the PTO-1050 do not agree.
- ☐ b. The name of the patentee on the patented file does not agree with that shown on the enclosed papers..

☐ 5. The record reveals that there is no power of attorney to ~~you in this case.~~ A written power or authorization from the patentee, or assignee, if any, must be submitted, before the request may be considered.

☐ 6. The request cannot be considered, because the paper indicated below was filed on ____________, AFTER payment of the issue fee: [See 37 CFR 1.313(B.].
- ☐ a. Amendment purported to be under Rule 312.
- ☐ b. Assignment.
- ☐ c. Priority papers.
- ☐ d. Other (identify) ____________.

☐ 7. Other: ____________

☐ A. PLEASE RETURN A COPY OF THIS LETTER TOGETHER WITH THE ENCLOSED PAPERS AS CORREECTED TO ENSURE EXPEDIENT ASSOCIATION WITH THE FILE

☐ B. Enclosed are copies of PTOL-1050 for use in typing the subject matter to be printed on the Certificate. This will avoid delay in handling request (See 862 O.G.2).

Decisions and Certificate of Correction Branch

FORM PTOL-396 (8/75)

ATTORNEY'S DOCKET NO.: S1022.81019US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Alexandre PONS and Christophe BERNARD		
Serial No.:	10/614,380	Patent No. 6,894,467 B2	
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ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Sir/Madam:

Patentee respectfully requests the correction of errors found in the above-captioned patent. Specifically, there are typographical errors in column 6 and 7 of issued U.S. Patent No. 6,894,467 B2.

As originally filed the paragraph on page 8, line 31 read as shown below:

> Comparator 50 comprises an input/output stage 4 and an output stage 5. Stage 4 comprises two differential branches, each comprised of a P-channel MOS transistor 61, 62 series connected with an N-channel MOS transistor 63, 64. The sources of transistors 61 and 62 are connected to an output terminal of a current source 60, an input terminal of which is connected to high supply Vdd. The sources of transistors 63 and 64 are connected to low supply GND. The gates of transistors 63 and 64 are interconnected. The gate of transistor 61 forms terminal I1 and receives reference voltage V1. The gate of transistor 63 is connected to its drain, that is, also to the drain of transistor 61. The gate of transistor 62 forms terminal **I2** and receives current voltage Vout across load 1 by a connection to output terminal OUT of the regulator. Connection point 65 of the drains of transistors 62 and 64 forms the output of input/output stage 4 of comparator 50. (Emphasis added)

However, the corresponding text found in column 6, on lines 25-28 reads as shown below:

Comparator 50 comprises an input/output stage 4 and an output stage 5. Stage 4 comprises two differential branches, each comprised of a P-channel MOS transistor 61, 62 series connected with an N-channel MOS transistor 63, 64. The sources of transistors 61 and 62 are connected to an output terminal of a current source 60, an input terminal of which is connected to high supply Vdd. The sources of transistors 63 and 64 are connected to low supply GND. The gates of transistors 63 and 64 are interconnected. The gate of transistor 61 forms terminal I1 and receives reference voltage V1. The gate of transistor 63 is connected to its drain, that is, also to the drain of transistor 61. The gate of transistor 62 forms terminal **12** and receives current voltage Vout across load 1 by a connection to output terminal OUT of the regulator. Connection point 65 of the drains of transistors 62 and 64 forms the output of input/output stage 4 of comparator 50. (Emphasis added)

No amendment was made by either the Examiner or Patentees to cause the reference character "I2" to be changed to "12" in column 6, line 51 of issued U.S. Patent No. 6,894,467.

As originally filed the paragraph on page 9, line 24 read as shown below:

Second differential comparator 51 is intended to control the regulation of the voltage at point MID. It provides on output terminal **O1** the control signal of gate **G1**. Second comparator 51 comprises two symmetrical differential branches, each formed of the series connection of an impedance 52, 53, preferably resistive, and of an N-channel MOS transistor 54, 55, respectively. The sources of transistors 54 and 55 are connected to the drain of an N-channel MOS transistor 56 having its source connected to ground GND. The gate of transistor 56 is connected to output 65 of input/output stage 4 and to the gate of transistor 10 of output stage 5 of first differential comparator 50. Accordingly, the operating point of the second differential comparator 51 depends on that of output stage 5 of first differential comparator 50. This enables stabilizing the control signal of gate G1 of transistor 32 at most at a required level, which depends on the level of the control signal of gate G2 of transistor 33 provided by first comparator 50. In particular, when load 1 is invalidated and transistor 33 is off, transistor 56 will be totally conductive and will enable a control of gate G1 capable of limiting voltage Vmid to half (Vdd/2) the high supply, as described previously in relation with Fig. 4. The gates of transistors 54 and 55 form, respectively, terminals **I3** and **I4** of application of voltages V2 and Vmid. (Emphasis added)

However, the corresponding text found in column 6, line 56 through column 7, line 20 reads as shown below:

> Second differential comparator 51 is intended to control the regulation of the voltage at point MID. It provides on output terminal **O1** the control signal of gate **GI**. Second comparator 51 comprises two symmetrical differential branches, each formed of the series connection of an impedance 52, 53, preferably resistive, and of an N-channel MOS transistor 54, 55, respectively. The sources of transistors 54 and 55 are connected to the drain of an N-channel MOS transistor 56 having its source connected to ground GND. The gate of transistor 56 is connected to output 65 of input/output stage 4 and to the gate of transistor 10 of output stage 5 of first differential comparator 50. Accordingly, the operating point of the second differential comparator 51 depends on that of output stage 5 of first differential comparator 50. This enables stabilizing the control signal of gate G1 of transistor 32 at most at a required level, which depends on the level of the control signal of gate G2 of transistor 33 provided by first comparator 50. In particular, when load 1 is invalidated and transistor 33 is off, transistor 56 will be totally conductive and will enable a control of gate G1 capable of limiting voltage Vmid to half (Vdd/2) the high supply, as described previously in relation with Fig. 4. The gates of transistors 54 and 55 form, respectively, terminals **13** and **14** of application of voltages V2 and Vmid. (Emphasis added)

No amendment was made by either the Examiner or Patentees to cause the reference characters"O1, G1, I3 and I4" (found on page 9, lines 16, 25 and page 10, line 5, respectively), to be changed to "01, GI, 13 and 14" (found in column 6, lines 51 and 66 and column 7, line 20 respectively) of issued U.S. Patent No. 6,894,467.

Support for the corrections to the reference numerals can be found in Fig. 5, where all of these reference characters, as they appear in the specification of the application as filed, can be found.

Patentees enclosed herein highlighted copies of pages 9 and 10 of the application as filed, Fig. 5 and columns 6 and 7 of issued U.S. Patent No. 6,894,467. Also enclosed is PTO form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Patentees respectfully submit that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on the 2 day of August, 2005.

Attorney Docket No.: S1022.80672US00
XNDD

Respectfully submitted,

Alexandre Pons et al., Applicant

By:

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PTO/SB/44 (04-04)
Approved for use through 04/30/2007
U.S. Patent and Trademark Office; US. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,894,467 B2

DATED : May 17, 2005

INVENTOR(S) : Alexandre Pons and Christophe Bernard

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 6, line 51 should read:
--forms terminal 12 and receives current voltage Vout across--

Col. 6, line 66 should read:
--output terminal O1 the control signal of gate GI. Second--

Col. 7, line 19 should read:
--minals 13 and 14 of application of voltages V2 and Vmid.--

MAILING ADDRESS OF SENDER

PATENT NO. 6,894,467

James H. Morris
Wolf, Greenfield & Sacks, P.C.
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Boston, Massachusetts 02210

AUG 1 2 2005

signals of gates G1 and G2 of transistors 32 and 33, respectively, to modify their transconductance.

The control signals of output stage 31 are generated by a control circuit 35. Circuit 35 modulates the control signal of gate G1 of transistor 32 to regulate the voltage at midpoint MID of the series connection of transistors 32 and 33 of output stage 31. It also modulates the control signal of gate G2 of transistor 32 to regulate output voltage Vout. Circuit 35 comprises an input/output stage (IN/OUT) 36 intended to generate the control signals and a reference stage (REF) 37. Input/output stage 36 comprises four input terminals I1, I2, I3, and I4 and two output terminals O1 and O2. Terminal I1 receives a voltage reference V1 for regulating output voltage Vout. Terminal I2 receives output voltage Vout. Terminal I3 receives a voltage reference V2 for regulating the voltage at midpoint MID. Terminal I4 receives voltage Vmid of midpoint MID by direct connection to this point. Output terminals O1 and O2 are respectively connected to gates G1, G2.

Regulation reference voltages V1 and V2 received on terminals I1 and I3 of stage 36, respectively, are provided by reference circuit (REF) 37 based on a variable D.C. voltage source 38 (Vreg). More specifically, to regulate midpoint MID to guarantee an equipartition of the voltages across each of the two transistors in series 32 and 33, regulation reference voltage V2 of midpoint MID is equal to half the sum of high supply voltage Vdd and of first regulation reference voltage V1 (V2=(Vdd+V1)/2). Source 38 thus directly provides, preferably, first reference voltage V1 (Vreg=V1), based on which circuit 37 provides second reference voltage V2 according to the preceding relation.

FIGS. 4A, 4B, 4C, and 4D respectively illustrate in timing diagrams the variation along time t of reference voltage V1 for regulating output voltage Vout of regulator 30 of circuit 3, of output voltage Vout, of reference voltage V2 for regulating the voltage of midpoint MID, and of current voltage Vmid at midpoint MID, that is, the drain voltage of transistor 32.

As regulator 30 is turned on, at a time t10, reference circuit 37 is validated by a turning-on of source 38 and generates regulation reference voltages V1 and V2. As illustrated in FIGS. 4A and 4C, regulation reference voltages V1 and V2 are, in a starting phase, (times t10 to t11), parallel ramps. Indeed, as indicated previously, to ensure a voltage distribution balance across transistors 32 and 33, it must be ensured that at any time the voltage at midpoint MID is equal to half the difference between high supply voltage Vdd and voltage Vout across load 1 (Vmid=(Vdd−Vout)/2). For this purpose, a reference voltage equal to half the sum of high supply voltage Vdd and of first reference voltage V1 must be applied. Upon variation of reference voltage V1 from a zero value to a nominal reference value Vref, control circuit 35 must be able to ensure such a condition. To enable linear follow-up, it is then preferable for reference voltage V1 to vary slowly rather than abruptly as in the case of a standard reference voltage (FIG. 2A).

As illustrated in FIG. 4B, in the starting phase, output voltage Vout follows, from time t10, first reference voltage V1 until it stabilizes at time t11 at nominal value Vref. Voltage Vmid at midpoint MID, illustrated in FIG. 4D, however decreases in a controlled manner from half the high supply voltage (Vdd/2) to the steady value (Vdd−Vref)/2. In nominal operation, between times t11 and t12, output voltage Vout and midpoint voltage Vmid are maintained steady by steady reference voltages V1 and V2. In a turn off control of load 1 at a time t12, to enable linear follow-up of second reference voltage V2, first reference voltage V1 is progressively brought down to zero along a ramp until a time t13. Supply Vdd then symmetrically distributes on transistors 32 and 33.

In nominal operation, (from t11 to t12), control circuit 35 ensures for any possible fluctuation of the power at the level of load 1 to translate as a variation in reference voltages V1 and V2 to restore the nominal operation and distribute the power variation symmetrically on the two power transistors 32 and 33. Thus, none of the two transistors 32 and/or 33 has to face an excessive drain/source voltage.

Power-up and power-off ramps of different respective slope have been shown in FIG. 4. More specifically, a faster power-off (t12–t13) than the power-up (t10–t11) has more particularly been shown. In practice, the slope of the ramps depends on the technical performances of the circuits and especially on the capacity of control circuit 35 to follow, transform and transmit the variation of first reference voltage V1. The slopes may be faster or slower than what is shown. Further, they may be symmetrical or exhibit an asymmetry which is the inverse of that shown, that is, the power-up may be faster than the power-off.

FIG. 5 schematically and partially illustrates the structure of an embodiment of the input/output stage 36 of a control circuit 35 of an output stage 31 of a regulator 30 according to the present invention.

Input/output circuit 36 with four inputs and two outputs is a differential comparator. More specifically, circuit 36 is formed of the association of a first differential comparator 50 and of a second differential comparator 51 interlaced as follows.

First comparator 50, delimited by a frame in dotted lines in FIG. 5, is intended to regulate output voltage Vout based on first reference voltage V1. Comparator 50 thus has a structure similar to that of a known differential comparator such as comparator 3 described in relation with FIG. 1. For clarity, the structure of comparator 50 is described hereafter by means of the same reference numerals as in FIG. 1.

Comparator 50 comprises an input/output stage 4 and an output stage 5. Stage 4 comprises two differential branches, each comprised of a P-channel MOS transistor 61, 62 series connected with an N-channel MOS transistor 63, 64. The sources of transistors 61 and 62 are connected to an output terminal of a current source 60, an input terminal of which is connected to high supply Vdd. The sources of transistors 63 and 64 are connected to low supply GND. The gates of transistors 63 and 64 are interconnected. The gate of transistor 61 forms terminal I1 and receives reference voltage V1. The gate of transistor 63 is connected to its drain, that is, also to the drain of transistor 61. The gate of transistor 62 forms terminal I2 and receives current voltage Vout across load 1 by a connection to output terminal OUT of the regulator. Connection point 65 of the drains of transistors 62 and 64 forms the output of input/output stage 4 of comparator 50.

Output stage 5 is formed of the series connection, between high supply Vdd and ground GND, of an impedance 9, preferably resistive (R), and of a an N-channel MOS transistor 10. The connection point of impedance 9 and of transistor 10 forms output terminal O2 providing the control signal of gate G2 of transistor 33. The gate of transistor 10 is connected to midpoint 65 of differential branch 62-64 of input stage 4.

Second differential comparator 51 is intended to control the regulation of the voltage at point MID. It provides on output terminal 01 the control signal of gate GI. Second comparator 51 comprises two symmetrical differential

branches, each formed of the series connection of an impedance 52, 53, preferably resistive, and of an N-channel MOS transistor 54, 55, respectively. The sources of transistors 54 and 55 are connected to the drain of an N-channel MOS transistor 56 having its source connected to ground GND. The gate of transistor 56 is connected to output 65 of input/output stage 4 and to the gate of transistor 10 of output stage 5 of first differential comparator 50. Accordingly, the operating point of the second differential comparator 51 depends on that of output stage 5 of first differential comparator 50. This enables stabilizing the control signal of gate G1 of transistor 32 at most at a required level, which depends on the level of the control signal of gate G2 of transistor 33 provided by first comparator 50. In particular, when load 1 is invalidated and transistor 33 is off, transistor 56 will be totally conductive and will enable a control of gate G1 capable of limiting voltage Vmid to half (Vdd/2) the high supply, as described previously in relation with FIG. 4. The gates of transistors 54 and 55 form, respectively, terminals 13 and 14 of application of voltages V2 and Vmid.

FIG. 6 schematically and partially shows an embodiment of a generator 37 of reference voltages V1 and V2. Reference circuit 37 is, according to an embodiment of the present invention, a resistive dividing bridge. The resistive bridge comprises the series connection between high supply rail Vdd and low supply rail GND of three successive resistors 71, 72, and 73. Connection point 74 of resistors 72 and 73 is the output terminal of a differential comparator 75 with two inputs and one output, for example, similar to comparator 3 of FIG. 1. The non-inverting input terminal of comparator 75 receives reference voltage Vreg for regulating output voltage Vout of regulator 30, for example, by a connection to source 38. The inverting input of comparator 75 is connected to output terminal 74. Thus, the first reference voltage called V1 is copied across resistor 73. By choosing resistors 71 and 72 of same values, the midpoint of these two resistors is controlled linearly by comparator 75 at the desired value V2 of half the sum of the supply voltage and of first reference voltage V1.

The present invention advantageously provides a linear power regulator that can be completely made with a standard low-voltage MOS manufacturing process and of small dimensions. Indeed, the replacing of the high-voltage MOS transistor of known regulators by two low-voltage transistors enables reducing the integration surface area. Further, the surface area increase of control part 35 with respect to the control circuit of a known regulator is negligible as compared to the gain in surface area linked to the power switch change.

Further, the linear regulator according to the present invention exhibits a waste voltage smaller than that of known regulators. As a non-limiting example, if high supply voltage Vdd is from 3.3 to 5.5 volts, each transistor 32 and 33 of output stage 31 of linear regulator 30 of the present invention is a standard MOS transistor capable of standing a drain/source voltage of approximately 2.5 volts. The waste voltage of the regulator is then reduced to values on the order of 200 mV.

Of course, the present invention is likely to have various alterations, modifications, and improvement which will readily occur to those skilled in the art. In particular, it should be noted that capacitor C (impedance 11) for stabilizing output voltage Vout has been described as functionally belonging to linear regulator 30. In practice, the capacitance of capacitor C is relatively high and varies according to the application, that is, to load 1. Capacitor C thus is, preferably, formed outside of an integrated circuit chip comprising the whole of regulator 30, and is directly assembled in parallel on load 1. Further, those skilled in the art will know how to modify the characteristics of the various components according to the used manufacturing process.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. A linear regulator having an output stage comprising first and second P-channel MOS transistors serially connected between a first D.C. supply terminal and an output terminal providing a regulated output voltage, and a circuit for controlling the first and second transistors capable of providing said first and second transistors with first and second control signals as a function of the output voltage and the voltage at the midpoint of the series connection.

2. The regulator of claim 1, wherein the control circuit comprises an input/output circuit and a reference circuit, the input/output circuit comprising:

- a first input, receiving a first voltage reference provided by said reference circuit;
- a second input, connected to said output terminal;
- a third input receiving a second voltage reference provided by said reference circuit;
- a fourth input connected to said midpoint;
- a first output connected to the gate of the first transistor; and
- a second output connected to the gate of the second transistor.

3. The method of claim 2, wherein the input/output circuit is a double differential comparator with four inputs and two outputs.

4. The regulator of claim 2, wherein the input/output circuit comprises first and second differential comparators with two inputs and two outputs, the input terminals of the first differential comparator being the first and second input terminals of the input/output circuit and its output being the second output of said input/output circuit; and the input terminals of the second differential comparator being the third and fourth input terminals of said input/output circuit and its output being the first output thereof.

5. The regulator of claim 4, wherein the first differential comparator comprises an input/output stage and an output stage, said input output stage comprising two differential branches, each of which comprises a P-channel MOS transistor connected in series with a first N-channel MOS transistor, the sources of the P-channel transistors being interconnected to an output terminal of a current source having an input terminal connected to said D.C. supply terminal, the sources of the first N-channel transistors being interconnected to a ground terminal, the gates of the N-channel MOS transistors being interconnected, the gates of the P-channel transistors forming the first and second input terminals of the input/output circuit, the gate of said first N-channel MOS transistor of the branch comprising the first input being connected to its drain, the midpoint of connection of the drains of the complementary transistors of the other branch being connected to the gate of a second N-channel MOS transistor connected, in said output stage, in series between the supply terminals, with a first impedance, the midpoint of the series connection of said first impedance and of the second transistor forming the output terminal of said first differential comparator.

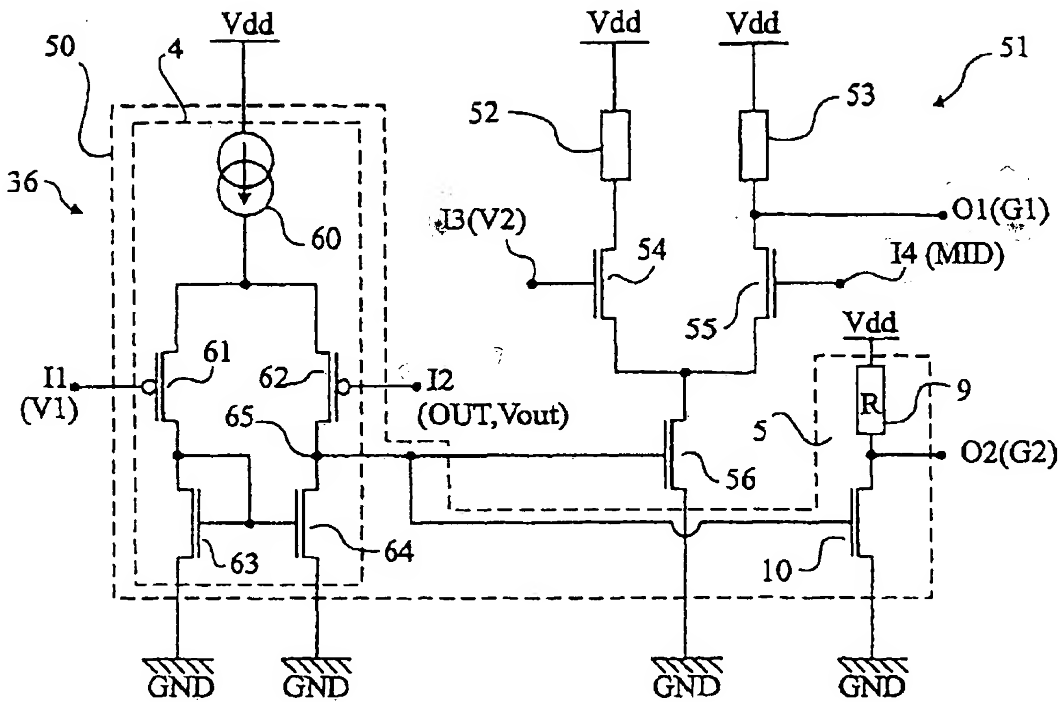
Vdd
50
4
36
60
Vdd
Vdd
52
53
51
I3(V2)
54
O1(G1)
I4 (MID)
55
Vdd
I1
(V1)
61
62
I2
(OUT,Vout)
65
9
R
5
O2(G2)
56
63
64
10
GND
GND
GND
GND

Fig 5

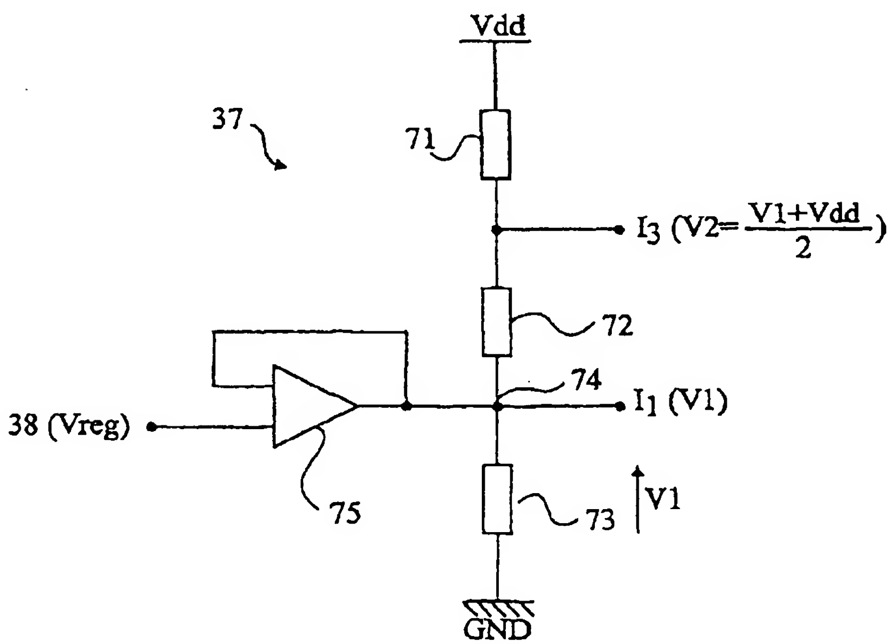
Vdd
37
71
I3 (V2= V1+Vdd / 2)
72
74
I1 (V1)
38 (Vreg)
75
73
V1
GND

Fig 6

differential comparator 50 and of a second differential comparator 51 interlaced as follows.

First comparator 50, delimited by a frame in dotted lines in Fig. 5, is intended to regulate output voltage Vout based on first reference voltage V1. Comparator 50 thus has a structure similar to that of a known differential comparator such as comparator 3 described in relation with Fig. 1. For clarity, the structure of comparator 50 is described hereafter by means of the same reference numerals as in Fig. 1.

Comparator 50 comprises an input/output stage 4 and an output stage 5. Stage 4 comprises two differential branches, each comprised of a P-channel MOS transistor 61, 62 series connected with an N-channel MOS transistor 63, 64. The sources of transistors 61 and 62 are connected to an output terminal of a current source 60, an input terminal of which is connected to high supply Vdd. The sources of transistors 63 and 64 are connected to low supply GND. The gates of transistors 63 and 64 are interconnected. The gate of transistor 61 forms terminal I1 and receives reference voltage V1. The gate of transistor 63 is connected to its drain, that is, also to the drain of transistor 61. The gate of transistor 62 forms terminal I2 and receives current voltage Vout across load 1 by a connection to output terminal OUT of the regulator. Connection point 65 of the drains of transistors 62 and 64 forms the output of input/output stage 4 of comparator 50.

Output stage 5 is formed of the series connection, between high supply Vdd and ground GND, of an impedance 9, preferably resistive (R), and of a an N-channel MOS transistor 10. The connection point of impedance 9 and of transistor 10 forms output terminal O2 providing the control signal of gate G2 of transistor 33. The gate of transistor 10 is connected to midpoint 65 of differential branch 62-64 of input stage 4.

Second differential comparator 51 is intended to control the regulation of the voltage at point MID. It provides on output terminal O1 the control signal of gate G1. Second comparator 51 comprises two symmetrical differential branches, each formed of the series connection of an impedance 52, 53, preferably resistive, and of an N-channel MOS transistor 54, 55, respectively. The sources of transistors 54 and 55 are connected to the drain of an N-channel MOS transistor 56 having its source connected to ground GND. The gate of transistor 56 is connected to output 65 of input/output stage 4 and to the gate of transistor 10 of output stage 5 of first differential comparator 50. Accordingly, the operating point of the second differential comparator 51 depends on

that of output stage 5 of first differential comparator 50. This enables stabilizing the control signal of gate G1 of transistor 32 at most at a required level, which depends on the level of the control signal of gate G2 of transistor 33 provided by first comparator 50. In particular, when load 1 is invalidated and transistor 33 is off, transistor 56 will be totally conductive and will enable a control of gate G1 capable of limiting voltage Vmid to half (Vdd/2) the high supply, as described previously in relation with Fig. 4. The gates of transistors 54 and 55 form, respectively, terminals I3 and I4 of application of voltages V2 and Vmid.

Fig. 6 schematically and partially shows an embodiment of a generator 37 of reference voltages V1 and V2. Reference circuit 37 is, according to an embodiment of the present invention, a resistive dividing bridge. The resistive bridge comprises the series connection between high supply rail Vdd and low supply rail GND of three successive resistors 71, 72, and 73. Connection point 74 of resistors 72 and 73 is the output terminal of a differential comparator 75 with two inputs and one output, for example, similar to comparator 3 of Fig. 1. The non-inverting input terminal of comparator 75 receives reference voltage Vreg for regulating output voltage Vout of regulator 30, for example, by a connection to source 38. The inverting input of comparator 75 is connected to output terminal 74. Thus, the first reference voltage called V1 is copied across resistor 73. By choosing resistors 71 and 72 of same values, the midpoint of these two resistors is controlled linearly by comparator 75 at the desired value V2 of half the sum of the supply voltage and of first reference voltage V1.

The present invention advantageously provides a linear power regulator that can be completely made with a standard low-voltage MOS manufacturing process and of small dimensions. Indeed, the replacing of the high-voltage MOS transistor of known regulators by two low-voltage transistors enables reducing the integration surface area. Further, the surface area increase of control part 35 with respect to the control circuit of a known regulator is negligible as compared to the gain in surface area linked to the power switch change.

Further, the linear regulator according to the present invention exhibits a waste voltage smaller than that of known regulators. As a non-limiting example, if high supply voltage Vdd is from 3.3 to 5.5 volts, each transistor 32 and 33 of output stage 31 of linear regulator 30 of the present invention is a standard MOS transistor capable of standing a